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L3	32	coverification	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/30 18:05
L4	72	co-verification	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/30 18:05
L5	6	4 and @ad<"19980301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/30 18:07
L6	215	co-simulation	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/30 18:07
L7	33	6 and @ad<"19980301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/30 18:20
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L8	26	codesign and @ad<"19980301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/30 18:23
L9	55	co-design and @ad<"19980301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/30 18:23

S95	2416	S93 and (wait adj state)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/31 17:52
S96	63	S95 and (processor adj wait adj state)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/31 18:23
S97	245	(memory adj simulat\$7) and @ad<"19980220"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/03/31 18:24
S98	32	("4130885" "4315315" "4455619" "4527249" "4584642" "4587625" "4677587" "4695968" "4725971" "4725975" "4744084" "4787062" "4827427" "4862347" "4882690" "4901260" "4918594" "4922445" "4937765" "5029102" "5062067" "5111413" "5151867" "5175843" "5198705" "5222030" "5313615" "5392227" "5528752" "5544067" "5559718" "5819063").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/03/31 18:26

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Your Search was:

Last Name = BUCKMASTER

First Name = MICHAEL

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09916148	Not Issued	030	07/25/2001	SYSTEM AND METHOD FOR TESTING AN EMBEDDED MICROPROCESSOR SYSTEM CONTAINING PHYSICAL AND/OR SIMULATED HARDWARE	BUCKMASTER, MICHAEL R.
09024324	6298320	150	02/17/1998	SYSTEM AND METHOD FOR TESTING AN EMBEDDED MICROPROCESSOR SYSTEM CONTAINING PHYSICAL AND/OR SIMULATED HARDWARE	BUCKMASTER, MICHAEL R.

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

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Last Name = BERGER

First Name = ARNOLD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09435002	Not Issued	161	11/05/1999	MULTI-CHIP IN-CIRCUIT EMULATOR MODULE AND EMULATOR SYSTEM USING SAME	BERGER PH.D, ARNOLD S.
09916148	Not Issued	030	07/25/2001	SYSTEM AND METHOD FOR TESTING AN EMBEDDED MICROPROCESSOR SYSTEM CONTAINING PHYSICAL AND/OR SIMULATED HARDWARE	BERGER, ARNOLD S.
07292590	5051888	250	12/30/1988	DATA PROCESSING SYSTEM FOR COORDINATING MEASUREMENT ACTIVITY UPON PLURALITY OF EMULATORS	BERGER, ARNOLD S.
07422877	Not Issued	161	10/17/1989	METHOD AND APPARATUS FOR COORDINATING MEASUREMENT ACTIVITY UPON A PLURALITY OF EMULATORS	BERGER, ARNOLD S.
07718728	5202976	150	06/21/1991	METHOD FOR SIMULTANEOUSLY BEGINNING EXECUTION OF USER CODE UPON A PLURALITY OF EMULATORS	BERGER, ARNOLD S.
08006571	Not Issued	161	01/21/1993	ANALYZER CONTROL BUS WITH SIGNAL LINE HAVING CONTEXT DEPENDENT MEANING	BERGER, ARNOLD S.
09024324	6298320	150	02/17/1998	SYSTEM AND METHOD FOR TESTING AN EMBEDDED MICROPROCESSOR SYSTEM CONTAINING PHYSICAL AND/OR SIMULATED HARDWARE	BERGER, ARNOLD S.

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De Michell, G.; Gupta, R.K.;
Proceedings of the IEEE
Volume 85, Issue 3, March 1997 Page(s):349 - 365
AbstractPlus References Full Text: PDF(252 KB) IEEE JNL</p> |
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Achterop, S.; Spaanenburg, L.;
EUROMICRO 97. 'New Frontiers of Information Technology'. Short Contributions., Proc
23rd Euromicro Conference
1-4 Sept. 1997 Page(s):208 - 214
AbstractPlus Full Text: PDF(468 KB) IEEE CNF</p> |
| <input type="checkbox"/> | <p>3. Transformational partitioning for co-design of multiprocessor systems
Marchioro, G.F.; Daveau, J.-M.; Jerraya, A.A.;
Computer-Aided Design, 1997. Digest of Technical Papers., 1997 IEEE/ACM Internatic
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Heinrich, M.; Ofelt, D.; Horowitz, M.A.; Hennessy, J.;
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Balboni, A.; Fornaciari, W.; Sciuto, D.;
Hardware/Software Co-Design, 1996. (Codes/CASHE '96), Proceedings., Fourth Intern
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- ☐ 10. **The design of mixed hardware/software systems**
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- ☐ 12. **Testability analysis of co-designed systems**
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Hartenstein, R.W.; Becker, J.; Kress, R.; Reinig, H.;
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Fishwick, P.A.;
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- ☐ 9. **Asynchronous parallel discrete event simulation**
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- ☐ 10. **Time-domain non-Monte Carlo noise simulation for nonlinear dynamic circuits w
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- ☐ 13. **A knowledge-based simulation environment for hierarchical flexible manufacturi**
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